



At the heart of our TRIUMPH Technology is our TRIUMPH Chip. In a 17x17 millimeter power-efficient 352-TFBGA chip we have packed impressive amount of state-of-the-art functions using 0.09 micron (90 nm) integrated circuit technology. The TRIUMPH chip has 216 (two hundred and sixteen) channels for tracking all types of GNSS signals. These 216 channels are grouped in three categories of channels, some with 5 and some with 10 correlators, optimized to track all types of GNSS signals.

The TRIUMPH Chip can track all existing satellite signals as well as all those planned for the future. This includes all GPS, GLONASS, Galileo, QZSS, WAAS, EGNOS, and Compass/Beidou signals.

Additionally these 216 channels are accompanied by the equivalent of 110,000 regular correlators for fast acquisition even when signal strength is very low.

Each channel is optimized to measure the most precise code, carrier and Doppler from each satellite system. The most advanced multipath reduction is also implemented for each channel. Each channel has 3-bit RF input and a tracking resolutions of 5 mm for code measurements and 0.005 mm for phase measurements.

The TRIUMPH Chip also includes a very powerful Floating Point Unit (FPU), 4 MB internal RAM power consumption and cost.

Harmonics of transmitters like TV and and block the reception. To defend TRIUMPH Chip has five sophisticated in five different signal bands, capable of to 60 dB.

Decoding the bit streams of GPS L5, Galileo, WAAS, EGNOS, and similar systems, which use Viterbi decoding schemes, are very computationally intensive. To facilitate this task we have implemented Viterbi decoder and cyclical redundancy check (CRC) module in the TRIUMPH Chip hardware. The implemented Viterbi decoder has 3-bit soft decision, decoding depth of 64 and capable of decoding frames of up to 512 bit with a decoding speed of 1 Mb/sec. It can support both stream and block modes. The CRC module has a polynomial length of up to 32.

TRIUMPH Chip also includes 40 flexible programmed RF input pins, three 1-PPS timing signal outputs, three Event inputs, and two embedded PLL-s.

The sophisticated power management implemented on the 90 nm technology reduces the power consumption of the chip to the range of 0.2 to 1 Watt depending on the modules activated.

Our TRIUMPH Chip not only offers impressive and unparalleled performance, it also provides for substantial reduction in manufacturing cost. It enables us to reduce the size and power consumption and offer products at lower cost. This is not a price war, it's a technology war, which we are back to fight for you!



microprocessor including a 220 MHz CPU with for on-chip data processing which reduces

radio stations may fall within the GPS band against such in-band interferences 64-th order adaptive anti jamming filters, suppressing multiple interferences by up

TRIUMPH[®] Chip

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GNSS DSP module

- GNSS signal processing section
 - Viterbi decoder & CRC section
 - CPU & FPU section
 - Memory section
 - PLL & I/O section
 - 216 channels for GNSS signal tracking (5 correlators per each channel)
 - Advanced multipath mitigation technique
 - 8-bit RF input
 - 5 mm code measurement resolution
 - 0.005 mm phase measurement resolution
- 216 GNSS channels of the TRIUMPH Chip consist of the following groups:
- 72 CAP channels, each with 5 correlators. Each can track GPS or GLONASS C/A, SBAS (WAAS, EGNOS, etc), QZSS C/A, GLONASS P, or any equivalent signal.
 - 48 PLC (96 normal) channels, each with 10 correlators). Each PLC channel can track GPS P1+P2, GPS L2C (both L2CM and L2CL), GPS L5 (both pilot and data), GPS/GLONASS C/A with special features for dual tracking. In fact each of the PLC channels are equivalent of two channels.
 - 48 memory code (MC) channels, each with 5 correlators. Each channel may track any arbitrary code (up to 16 Mb length) including BOC and Alt-BOC modulation, for GPS L1C, Galileo, Compass/Beidou, etc.

Fast Acquisition module

- Equivalent to up to 110,000 regular correlators.
- 0.01 sec for complete frequency/delay search of one GPS/GLONASS/Galileo satellite under normal conditions.
- Sensitivity: down to 20 dB*Hz carrier-to-noise ratio (equivalent to -150 dBm signal power).

- Five 64-th order adaptive anti jamming filters capable to suppress multiple narrowband and wideband interferences by up to 60 dB
- 40 flexible programmed RF input pins
- Three 1-PPS outputs
- Three Event inputs

Embedded processor module

- 32-bit CPU compliant with the SPARC V8 architecture.
- 64-bit FPU compliant with IEEE 754 standard.
- Up to 220 MHz CPU/FPU clock speed.
- 128 KB instruction/data cache size.
- Memory Management Unit.
- 4 MB internal RAM.
- Up to 9 UARTs.
- Up to 5 advanced SPIs (four-wire serial with master/slave mode).
- Up to 3 CAN 2.0 controllers.
- Up to 21 PWM (pulse-width modulation) outputs.
- Up to 67 general purpose input/output pins.
- External bus supports up to 512 MB SDRAM, 128 MB SRAM, 128 MB PROM and memory mapped I/O devices.

Viterbi/CRC module

- For WAAS/EGNOS decoding
- Viterbi decoder: 3-bit soft decision, up to 512 bit frame, decoding depth – 64, up to 1 Mb/sec decoding speed, support of both stream and block modes.
- CRC module: polynomial length – up to 32.
- 2 embedded PLL's.



Specifications are subject to change without notice.



JAVAD GNSS
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